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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,743	08/19/2003	Seiji Narui	501.35152CC3	3820

20457 7590 09/08/2004

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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,743	NARUI ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☒ Claim(s) *6-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *19 August 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 4, and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Kajigaya (USPN 5,604,365).

4. In reference to claim 1, Kajigaya et al. (USPN 5,604,365, hereinafter referred to as the "Kajigaya" reference) discloses a similar device. Figure 36A of Kajigaya discloses a semiconductor integrated circuit device with a first region while figure 36B shows a second region of the same device. There are first MISFETs formed in the first region. There are second MISFETs formed in the second region. The second MISFETS have a gate electrode (5) and impurity regions (6). There is a first insulating layer (9) formed over the first and second

MISFETs. There are wordlines (4) formed over the first region. There are bitlines (10) formed over the wordlines (4) and the first insulating layer (9). Each of the first MISFETs is included in an individual one of a plurality of memory cells. Each of the memory cells is connected to a bitline (10) and a wordline (4). A second insulating layer (13A) is formed over the bitlines (10) and the first insulating layer (9). The first (9) and second (13A) insulating layers have holes with plugs (24, 25). In figure 36B, a wiring layer (15', 16, 23) is formed over the second insulating layer (13A) and is electrically connected to the impurity regions (6) of the second MISFETs by way of the plugs (24, 25).

5. In reference to claim 4, Kajigaya (USPN 5,604,365) discloses a similar device. Figure 36A of Kajigaya discloses a semiconductor integrated circuit device with a first region while figure 36B shows a second region of the same device. There are first MISFETs with source and drain regions (6) formed in the first region. There are second MISFETs with source and drain regions (6) formed in the second region. The second MISFETS have a gate electrode (5) and impurity regions (6). There is at least one bitline (10) formed over the first region. There is at least one wordline (4) formed in the first region. There is at least one capacitor element (15, 18, 19) formed over one of the bitlines (10). Each of the first MISFETs is included in an individual one of a plurality of memory cells. Each of the memory cells is coupled to a respective wordline (4), a respective bitline (10), and a capacitor element (15, 18, 19). There is a first insulating film (9) formed between the first MISFETs and at least one bitline (10). A second insulating film (13A) is formed over the first insulating film (9) and is

interposed between at least one bitline (10) and at least one capacitor element (15, 18, 19). Each of the bitlines (10) is connected to one of the source and drain regions (6) of the first MISFETs by a first plug (24) formed in the first insulating film (9). Each of the capacitor elements (15, 18, 19) is connected to one of the source and drain regions (6) of the first MISFETs by a second plug (25) formed in the second insulating film (13A) and another of the first plugs (24). In figure 36B, a wiring layer (15', 16, 23) is formed over the second insulating layer (13A) and is electrically connected to the impurity regions (6) of the second MISFETs by way of third plugs (24, 25).

6. In reference to claim 5, the first plug (24) is made of polysilicon (column 16, lines 3-10).

7. Claims 1, 2, and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Takaishi (USPN 5,726,083).

8. In reference to claim 1, Takaishi (USPN 5,604,365) discloses a similar device. Figure 2C of Takaishi discloses a semiconductor integrated circuit device with a first region (2) and a second region (3). There are first MISFETs formed in the first region. There are second MISFETs formed in the second region. The second MISFETS have a gate electrode (3d) and impurity regions (3f, 3g, 3i, 3j). There is a first insulating layer (4a) formed over the first and second MISFETs. There are wordlines (WL2, WL3, WL4) formed over the first region. There are bitlines (BL1, BL2) formed over the wordlines (WL2, WL3, WL4) and the first insulating layer (4a). Each of the first MISFETs is included in an individual one of a plurality of memory cells. Each of the memory cells is

connected to a bitline (BL1) and a wordline (WL1, WL2). A second insulating layer (4b) is formed over the bitlines (BL1, BL2) and the first insulating layer (4a). The first (4a) and second (4b) insulating layers have holes with plugs (6a, 6b). A wiring layer (7) is formed over the second insulating layer (4b) and is electrically connected to the impurity regions (3f, 3g, 3i, 3j) of the second MISFETs by way of the plugs (6a, 6b).

9. With regard to claims 2 and 3, the plugs are made of the built-up films (column 1, lines 5-24) of titanium nitride (5a) and tungsten (6a, 6b).

Allowable Subject Matter

10. Claims 6-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which teaches a semiconductor memory device structure with peripheral and memory sections having the exact barrier film plug structure which is in contact with a source or a drain region of a transistor in combination with the relative positions of the bitlines, wordlines, and capacitors as suggested by the applicant.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

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